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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,988	KIM ET AL.	
	Examiner	Art Unit	
	PHYOWAI LIN	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 3-6 and 8-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Ido et al. (US Pub Number 2002/0181853) and Nakanishi et al. (US Pub Number 2002/0071641).

Regarding to claim 1, applicant's admitted prior art disclose an optical transceiver (see FIG.1 prior art) comprising:

a photoelectric transducer implemented on a substrate (see FIG.1 prior art where in photoelectric transducer 1200 implements on a substrate 1300) and having a light transmitting device (a light transmitting device 1210) for converting an electrical signal into a light signal (see description of prior art page 4, lines 1-3 and FIG.1), a high-speed signal line (a high-speed signal line 1220) for the light transmitting device (see description of prior art page 4, lines 3-4 and FIG.1), a bias line (a bias line 1230) for the light transmitting device spaced from the high speed signal line for the light transmitting device (see description of prior art page 4, lines 4 and FIG.1where in there is a space apart between the high-speed signal line 1220 and the bias line 1230) ,a light receiving device (a light receiving device 1260) for converting the light signal into the electrical signal (see description of prior art page 4, lines 6-7 and FIG.1) , a high-speed signal line

(a high-speed signal line 1270) for the light receiving device (see description of prior art page 4, lines 7-8 and FIG.1) , a bias line (a bias line 1280) for the light receiving device spaced from the high speed signal line for the light receiving device (see description of prior art page 4, lines 8-9 and FIG.1where in there is a space apart between the high-speed signal line 1270 and the bias line 1280),

a light signal transmitter (a light signal transmitter 1100) connected to the photoelectric transducer (photoelectric transducer 1200), transmitting a light signal received from an optical fiber (an optical fiber 1700) to the light receiving device (light receiving device 1260), and transmitting a light signal generated from the light transmitting device (light transmitting device 1210) to the optical fiber (see description of prior art page 3, paragraph [0008] and FIG.1);

Even though applicant's prior art disclose optical transceiver module with high-speed signal lines and bias lines for both light transmitting device and light receiving device and central ground lines 1290, applicant prior art fails to specifically disclose the first dummy ground line with lead pin and second ground line with lead pin locate adjacent to and spaced from the high-speed signal lines 1220 and 1270 of both light transmitting device and light receiving device.

Ido et al. disclose a first dummy ground line (ground pins 6-1 and 6-3-see [0049] line16 and FIG.2) located adjacent to and spaced from the high-speed signal line (a microstrip line 3-9-see [0049] lines 5-10 and FIG.2 where in microstrip line 3-9 connects with lead pin 6-2 for permitting high-speed driving signal to the transmitting element 9) for the light transmitting device (see FIG.2 where in ground pin 6-3 is located adjacent

to and spaced from the high-speed signal line with lead pin 6-2 of the light transmitting device), and a second dummy ground line (ground pins 6-2 and 6-4-see [0079] line 8-9 and FIG.9) located adjacent to and spaced from the high-speed signal line (a strip line 3-9-see [0079] line 7and FIG.9) for the light receiving device (see FIG.9 where in ground pin 6-4 is located adjacent to and spaced from the high-speed signal line with lead pin 6-3 of the light receiving device);

wherein the space between the high-speed signal line (microstrip line 3-9 with lead pin 6-2) for the light transmitting device and the first dummy ground line (ground pins 6-1) is less than or equal to the space between the high-speed signal line for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device (see FIG.2 where in the distance between a microstrip line 3-9 with lead pin 6-2 and ground pin 6-1 is less than the distance between a microstrip line 3-9 with lead pin 6-2 and electrode pattern 3-11 with lead pin 6-4);and the space between the high-speed signal line (strip line 3-9 with lead pin 6-3) for the light receiving device and the second dummy ground line (ground pin 6-4) is less than or equal to the space between the high-speed signal line for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 12-15 and FIG.9) for the light receiving device (see FIG.9 in which the distance between a strip line 3-9 with lead pin 6-4 and ground lead 6-4 is smaller than the distance between the perimeter of a strip line 3-9 with lead pin 6-3 and the electrode pattern 3-12 with lead pin 6-5) and

whereby the first and second dummy lines respectively absorb spurious noise emitted from the respective high-speed signal lines (see paragraph [0071], lines 9-12 and paragraph [0003], lines 3-8 where in the ground pins which have function of electromagnetic shield can reduce the noise from the high speed signal line which is built in optical transceiver module).

Additionally, Nakanishi et al. also teaches that when metal shield plate is grounded to the ground pin, the ground pin can absorb the electromagnetic noise, which cause electric cross talk for the optical transceiver (see paragraph [0007], lines 1-10).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 3, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, Ido et al. disclose the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 with lead pin 6-2 and the electrode pattern 3-11 with lead pin 6-4); and

the second dummy ground line (lead 6-4-see [0079] lines 8-9 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 12-15 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 with lead pin 6-3 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 4, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, applicant's admitted prior art further discloses the optical transceiver including wherein the light transmitting device is a laser diode (see page 4, lines 1-3 where in a laser diode inherently implement inside the light transmitting device 1210 for converting the electrical signal into the light signal) and the light receiving device is a photo diode (see page 4, lines 6-7 where in a photo diode inherently implement inside the light receiving device 1260 for converting the light signal into the electrical signal).

Regarding to claim 5, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, applicant's admitted prior art further discloses the optical transceiver including where in the light signal transmitter is composed of a planner lightwave circuit (PLC) (see page 2, paragraph [0004] lines 1-3 and FIG.1).

Regarding to claim 6, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, Ido et al. further discloses the optical transceiver including: wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5-10 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 with lead pin 6-2 is

placed between the ground pin 6-1 and the electrode pattern 3-11 with lead pin 6-4) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] lines 12-15 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 with lead pin 6-3 is placed between around the perimeter of ground lead 6-2 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 8, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 6). In addition, both applicant's admitted prior art and Ido et al. disclose the optical transceiver including:

Ido et al. disclose wherein the first (ground pin 6-1-see [0049] line16 and FIG.2) and the second dummy ground lines (lead 6-2-see [0079] line 8 and FIG.9) are located

outside the photoelectric transducer (see FIG 2 and FIG 9 in which both ground lines are placed outside the LD module and PD module); and

Applicant's admitted prior art disclose the bias lines (bias lines 1230 and 1280-see FIG.1 prior art) for the light transmitting device and the light receiving device are located inside the photoelectric transducer (see FIG.1 prior art both bias lines 1230 and 1280 for light transmitting device 1210 and light receiving device 1260 are located inside the photoelectric transducer 1200).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. with Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 9, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, applicant's admitted prior art discloses the optical transceiver including: wherein the photoelectric transducer further comprises a monitor photo detector (MPD) signal line for monitoring optical power of the light transmitting device (see page 4, lines 5-6 and FIG.1 prior art).

Regarding to claim 10, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 9). In addition, Ido et al. disclose the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 with lead pin 6-2 and the electrode pattern 3-11 with lead pin 6-4); and

the second dummy ground line (lead 6-4-see [0079] lines 8-9 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 12-15 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 with lead pin 6-3 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to

particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 11, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 9). In addition, applicant's admitted prior art further discloses the optical transceiver including wherein the light transmitting device is a laser diode (see page 4, lines 1-3 where in a laser diode inherently implement inside the light transmitting device 1210 for converting the electrical signal into the light signal) and the light receiving device is a photo diode (see page 4, lines 6-7 where in a photo diode inherently implement inside the light receiving device 1260 for converting the light signal into the electrical signal).

Regarding to claim 12, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 9). In addition, applicant's admitted prior art further discloses the optical transceiver including where in the light signal transmitter is composed of a planner lightwave circuit (PLC) (see page 2, paragraph [0004] lines 1-3 and FIG.1).

Regarding to claim 13, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 9). In addition, Ido et al. further discloses the optical transceiver including: wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5-10 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049]

line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 with lead pin 6-2 is placed between the ground pin 6-1 and the electrode pattern 3-11 with lead pin 6-4) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] lines 12-15 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 with lead pin 6-3 is placed between around the perimeter of ground lead 6-2 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 14, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 13). In addition, Ido et al. further discloses the optical transceiver including: wherein the space between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light

transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) is less than or equal to the space between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device (see FIG.2 in which the space between a microstrip line 3-9 with lead pin 6-2 and ground pin 6-1 is less than the space between a microstrip line 3-9 with lead pin 6-2 and electrode pattern 3-11 with lead pin 6-4); and

the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) is less than or equal to the space between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device (see FIG.9 in which the space between a strip line 3-9 of lead pin 6-3 and ground lead 6-2 is less than the space between the perimeter of a strip line 3-9 with lead pin 6-3 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all

signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 15, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 13). In addition, applicant's admitted prior art and Ido et al. both disclose the optical transceiver including:

Ido et al. disclose wherein the first (ground pin 6-1-see [0049] line16 and FIG.2) and the second dummy ground lines (lead 6-2-see [0079] line 8 and FIG.9) are located outside the photoelectric transducer (see FIG 2 and FIG 9 in which both ground lines are placed outside the LD module and PD module); and

Applicant's admitted prior art disclose the bias lines (bias lines 1230 and 1280-see FIG.1 prior art) for the light transmitting device and the light receiving device are located inside the photoelectric transducer (see FIG.1 prior art both bias lines 1230 and 1280 for light transmitting device 1210 and light receiving device 1260 are located inside the photoelectric transducer 1200).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. with Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all

signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 16, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 1). In addition, both applicant's admitted prior art and Ido et al. disclose the optical transceiver including:

Applicant's admitted prior art disclose a package encapsulant (a package encapsulant 1500-see FIG.2 prior art) attached to the substrate (see FIG.2 prior art where in the package encapsulant 1500 is implemented on the substrate 1300);

a leadframe pad (a leadframe pad 1400) located inside the package encapsulant (see FIG.2 prior art where in the leadframe pad 1400 is implemented on the package encapsulant 1500).

Ido et al. disclose a plurality of leadframes (lead pins 6-1 through 6-8-see FIG.2 and FIG.9) connected to the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device, the bias line (electrode pattern 3-11-see [0070] line 4 and FIG.2) for the light transmitting device, the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device, the bias line (the electrode pattern 3-12-see [0079] line 14 and FIG.9) for the light receiving device, the first dummy ground line (ground pins 6-1,6-3) , the second dummy ground line (group pins 6-2, 6-4) and the leadframe pad (the electrode pattern 3-0-see[0051] line 7 and FIG.1) and also (see FIG.2 and FIG.9 where in the lead pins are connected to microstrip line 3-9, electrode pattern 3-11, a strip line 3-9 ,the electrode pattern 3-12 and ground pins 6-1,6-3,6-2,6-4) , respectively.

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. with Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 17, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 16). In addition, Ido et al. disclose the optical transceiver includes:

wherein the first dummy ground line (ground pin 6-3-see [0049] line16 and FIG.2) is located between the high-speed signal line (a microstrip line 3-9-see [0049] line5 and FIG.2) for the light transmitting device and the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device (see FIG.2 in which the ground pin 6-3 is placed between a microstrip line 3-9 with lead pin 6-2 and the electrode pattern 3-11 with lead pin 6-4); and

the second dummy ground line (lead 6-4-see [0079] lines 8-9 and FIG.9) is located between the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device and the bias line (the electrode pattern 3-12-see [0079] line

12-15 and FIG.9) for the light receiving device (see FIG.9 in which lead 6-4 is placed between around the perimeter of a strip line 3-9 with lead pin 6-3 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

Regarding to claim 18, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 16). In addition, applicant's admitted prior art further discloses the optical transceiver including wherein the light transmitting device is a laser diode (see page 4, lines 1-3 where in a laser diode inherently implement inside the light transmitting device 1210 for converting the electrical signal into the light signal) and the light receiving device is a photo diode (see page 4, lines 6-7 where in a photo diode inherently implement inside the light receiving device 1260 for converting the light signal into the electrical signal).

Regarding to claim 19, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 16). In addition, applicant's

admitted prior art further discloses the optical transceiver including where in the light signal transmitter is composed of a planner lightwave circuit (PLC) (see page 2, paragraph [0004] lines 1-3 and FIG.1).

Regarding to claim 20, applicant's admitted prior art, Ido et al. and Nakanishi et al. discloses everything claimed as applied above (see claim 16). In addition, Ido et al. further discloses the optical transceiver including: wherein the high-speed signal line (a microstrip line 3-9-see [0049] line5-10 and FIG.2) for the light transmitting device is located between the bias line (electrode pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device and the first dummy ground line (ground pin 6-1-see [0049] line16 and FIG.2) and also (see FIG2 in which a microstrip line 3-9 with lead pin 6-2 is placed between the ground pin 6-1 and the electrode pattern 3-11 with lead pin 6-4) ; and

the high-speed signal line (a strip line 3-9-see [0079] line 7 and FIG.9) for the light receiving device is located between the bias line (the electrode pattern 3-12-see [0079] lines 12-15 and FIG.9) for the light receiving device and the second dummy ground line (lead 6-2-see [0079] line 8 and FIG.9) and also (see FIG.9 in which a strip line 3-9 with lead pin 6-3 is placed between around the perimeter of ground lead 6-2 and the electrode pattern 3-12 with lead pin 6-5).

Therefore, it would have been an obviousness to combine the applicant's admitted prior art with Ido et al. and Nakanishi et al. for the purpose of implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines and ground lines with each assigned to particular

lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable, portable and reducing cross talk integrated optical transceiver circuit.

3. **Claims 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Ido et al. (US Pub Number 2002/0181853) and Nakanishi et al. (US Pub Number 2002/0071641) as applied to claim 1,respectively, above and further in view of Ido et al. (US Pub Number 2003/0194192).

Regarding to claim 2, applicant's admitted prior art, Ido et al. and Nakanishi et al. disclose everything claimed as applied above (see claim 1). However they fail to disclose what is the silicon substrate made of for better operating in optical communication.

Ido et al. (US Pub Number 2003/0194192) teaches the optical transceiver includes wherein the substrate (see [0027] line 15) is composed of a silicon substrate (see [0027] line 16) having a silicon oxide film (see [0027] line 16).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ido et al.'s invention as making the silicon substrate with the silicon oxide film on top of silicon substrate instead of using other chemical materials because insulation film of silicon oxide would not allow the current flow in the electrode of the photodiode and silicon oxide film itself has its own capacitance.

Response to Amendment

4. Applicant's arguments filed January 04, 2008 have been fully considered but they are not persuasive.

5. With respect to claims 1, 3-6 and 8-20, applicant argues that Examiner asserts that Ido discloses wherein the space between the high-speed signal line for the light transmitting device and the first dummy ground line (6-1) is less than or equal to the space between the high-speed signal line for the light transmitting device and the bias line (electrode pattern 3-11) for the light transmitting device, wherein the distance between microstrip line 3-9 with lead pin 6-2 and ground pin 6-1 is less than the distance between a microstrip line 3-9 with lead pin 6-2 and electrode pattern 3-11. Notwithstanding the assertions of the Examiner, Applicants respectfully submit that Ido fails to disclose dummy ground lines either on the substrate sub-mount 8 or on main body 2. Furthermore, not only do Applicants submit that ground pins 6-1 is not a dummy ground line, electrode pattern 3-11 fails to disclose a bias line, as recited in claim 1. Indeed, electrode pattern 3-11 is a ground for the light receiving device and therefore cannot correspond to any component of the light transmitting device, let alone the bias line for the light transmitting device.

In response, Ido et al. clearly disclose the space between the high-speed signal line (microstrip line 3-9 with lead pin 6-2) for the light transmitting device and the first dummy ground line (ground pins 6-1) is less than or equal to the space between the high-speed signal line for the light transmitting device and the bias line (electrode

pattern 3-11-see [0070] lines 1-4 and FIG.2) for the light transmitting device (see FIG.2 where in the distance between a microstrip line 3-9 with lead pin 6-2 and ground pin 6-1 is less than the distance between a microstrip line 3-9 with lead pin 6-2 and electrode pattern 3-11 with lead pin 6-4).Even though, Ido et al. disclose the ground pin without showing explicitly with dummy ground lines either on the substrate sub-mount 8 or on main body 2 in FIG.2, applicant's admitted prior art teaches the ground line 1290 on the substrate 1300 with ground lead frame (see applicant's admitted prior art FIG.1).Therefore, applicant's admitted prior art covers the deficiencies of the Ido et al. by teaching ground line 1290 on the substrate 1300 with ground lead frame.

Further more, teaching electrode pattern 3-11 in Ido et al. is not a ground for the light receiving device and Ido et al. clearly disclose the electrode pattern 3-11 for the bias line for the light transmitting device (see paragraph [0070] and FIG.2 where in using electro pattern 3-11 for measuring the photocurrent of optical output of the light transmitting module).

6. With respect to claims 1, 3-6 and 8-20, applicant further argues that because Ido fails to disclose any benefit of any special spacing between the leads, Applicants respectfully submit that the asserted combination of references is improper, and appears to be based on hindsight reasoning. Applicants respectfully submit that neither AAPA nor Ido suggest the desirability of combining such teachings. It is improper to use the claimed invention as an instruction manual to piece together the teachings of the prior art so that the claimed invention is rendered obvious. The Office Action appears to use improper hindsight reconstruction to pick and choose among isolated disclosures to

suggest a special arrangement of the bias lines, the high-speed signals and the dummy grounds of the AAPA. Because Ido fails to disclose dummy lines on the substrate; bias lines on the substrate; and further fails to disclose, teach, or suggest the specific arrangement between the high-speed signal lines, dummy ground lines, and bias lines, Ido cannot be relied upon to remedy the deficiencies of APAA to render claim 1 obvious.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In particularly, base on examiner explanation presented above , it would have been an obvious to one of the ordinary skills in the art to combine the applicant's admitted prior art with the teaching of Ido et al. for implementing Ido et al's invention of optical transceiver module which teaches design for space between bias lines, high-speed signal lines, ground pin with each assigned to particular lead pins to applicant's admitted prior art invention of optical transceiver module which has bias lines, high-speed signal lines and central ground lines with each assigned to particular lead pins because it would allow the optical transceiver module having all signal lines on one substrate with assigned lead pin and space design between them for making reliable,

portable, less cost and reducing electromagnetic noise emitted from integrated optical transceiver circuit.

7. With respect to claims 1, 3-6 and 8-20, applicant further argues that the examiner further cites Nakanishi to disclose that when a metal shield plate is grounded to the ground pin, the ground pin can absorb electromagnetic noise. Notwithstanding any disclosure of Nakanishi regarding the grounding of a metal shield, Applicants respectfully submit that Nakanishi fails to remedy the deficiencies of the AAPA and Ido as presented above.

In response, Nakanishi et al. teaches that when metal shield plate is grounded to the ground pin, the ground pin can absorb the electromagnetic noise, which cause electric cross talk for the optical transceiver (see paragraph [0007], lines 1-10). Therefore, Nakanishi does not fail to cure the deficiencies of the AAPA and Ido et al. as presented above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571)270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PWL 03/18/08

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